IN THE CLAIMS

Please amend the claims as follows.

For the Examiner's convenience, a list of all claims is included below.

1-22 (Cancelled)

23. (Original) The apparatus of claim 21 wherein the chip is a personal computer chipset.

24-28 (Cancelled)

29. (Original) The apparatus of claim 27 wherein the chip is a personal computer chipset.

30. (Original) An apparatus comprising:

an operating system to request a chip to start a time counter prior to entering a reduced power consumption state; and

the chip to start the time counter.

31. (Original) The apparatus of claim 30 wherein the operating system further operates to request the chip to halt the time counter.

32. (Original) The apparatus of claim 30 wherein the chip further operates to halt the time counter.

33. (Original) The apparatus of claim 30 wherein the time counter comprises a reduced power consumption state duration.

34. (Original) The apparatus of claim 30 wherein the chip is a personal computer chipset.

35. (Previously Presented) The apparatus of claim 30 wherein the reduced power consumption state is a C1 power state.

36-40 (Canceled)

41. (Original) An apparatus comprising:

means for starting a time counter;

means for entering a reduced power consumption state;

means for halting the time counter prior to an execution of an interrupt routine; and

means for exiting the reduced power consumption state.

42. (Original) The apparatus of claim 41 wherein the reduced power consumption state is a C1 power state.

43. (Original) The apparatus of claim 41 wherein the means for starting the time counter further comprise means for requesting a chip to start the time counter.

44. (Original) The apparatus of claim 41 wherein the means for halting the time counter further comprise means for requesting a chip to halt the time counter.

45. (Original) An apparatus comprising:

means for storing a time of entering a reduced power consumption state in a chip;

means for storing a time of exiting the reduced power consumption state in the chip prior to an execution of an interrupt routine; and

means for automatically calculating a reduced power consumption state duration.

46. (Original) The apparatus of claim 45 wherein the reduced power consumption state is a C1 power state.

47. (Original) The apparatus of claim 45 wherein the chip is a personal computer chipset.

48. (New) The method of claim 45 wherein both the means for storing are located in a chipset.

49. (New) A method comprising:

starting a time counter;

entering a reduced power consumption state;

halting the time counter prior to an execution of an interrupt routine; and

exiting the reduced power consumption state.

50. (New) The method of claim 49 wherein the starting the time counter comprises requesting a chip to start a time counter.

51. (New) The method of claim 49 wherein the halting the time counter comprises requesting a chip to halt the time counter.

52. (New) The method of claim 50 wherein the chip is a personal computer chipset.

53. (New) The method of claim 51 wherein the chip is a personal computer chipset.

54. (New) The method of claim 49 wherein the exiting the reduced power consumption state comprises executing the interrupt routine.

55. (New) The method of claim 49 wherein the time counter comprises a reduced power consumption state duration.

56. (New) The method of claim 49 wherein the reduced power consumption state is a C1 power state.

57. (New) A method comprising:

storing a time of entering a reduced power consumption state in a chip;

storing a time of exiting the reduced power consumption state in the chip prior to an execution of an interrupt routine; and

automatically calculating a reduced power consumption state duration.

58. (New) The method of claim 57 wherein the storing the time of entering the reduced power consumption state comprises storing the time of entering in a register.

59. (New) The method of claim 57 wherein the storing the time of exiting the reduced power consumption state comprises storing the time of exiting in a register.

60. (New) The method of claim 57 wherein the automatically calculating the reduced power consumption state duration is performed by the chip.

61. (New) The method of claim 60 wherein the chip is a personal computer chipset.

62. (New) The method of claim 57 wherein the reduced power consumption state is a C1 power state.